108 年 6 月　不通過 學術審查

年　　級：博 七 （101 博士班入學）

著作列表

Papers currently under review:

Journal paper

1. **學生 A**, 共同作者, 共同作者, "A Virtualization-Assisted Full-System Simulation Approach for the Verification of System Inter-Component Interactions." IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, (TCAD)

Published papers:

Journal Papers

1. 共同作者, **學生 A,** 共同作者, 共同作者, 共同作者, "Highly Efficient and Effective Approach for Synchronization-Function-Level Parallel Multicore Instruction-Set Simulations." IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 34.11 (2015): 1822-1835.

Conference Papers

1. **學生 A**, 共同作者, 共同作者, and 共同作者, "A Highly Efficient Virtualization-Assisted Approach for Full-System Virtual Prototypes," Workshop on Synthesis And System Integration of Mixed Information technologies (SASIMI) 2018.
2. 共同作者, **學生 A**, 共同作者 and 共同作者, "A Reuse-Distance Based Approach for Early-Stage Multi-level Cache Design Optimization," Workshop on Synthesis And System Integration of Mixed Information technologies (SASIMI) 2018
3. **學生 A**, 共同作者, 共同作者, and 共同作者, "A Highly Efficient Full-System Virtual Prototype Based on Virtualization-Assisted Approach," Design, Automation and Test in Europe Conference (DATE) 2018
4. 共同作者, **學生 A**, 共同作者, 共同作者, "A Data Effect Aware Microcomponent-Based Estimation Approach for Accurate System-Level Memory Device Power Evaluation," Workshop on Synthesis And System Integration of Mixed Information technologies (SASIMI) 2016

5. 共同作者, 共同作者, **學生 A**, 共同作者, "An Accurate Crowdsourcing-based Adaptive Fall Detection Approach Using Smart Devices," IEEE International Conference on Healthcare Informatics (ICHI) 2016
6. 共同作者, **學生 A**, 共同作者, and 共同作者, "An Accurate and Flexible Early Memory System Power Evaluation Approach Using a Microcomponent Method," International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS) 2016
7. **學生 A**, 共同作者, 共同作者, "An Effective Timing-Coherent Transactor Generation Approach for Mixed-level System Simulations," Workshop on Synthesis And System Integration of Mixed Information technologies (SASIMI) 2015
8. 共同作者, **學生 A**, 共同作者, "Automatic Timing-Coherent Transactor Generation for Mixed-level Simulations," Asia and South Pacific Design Automation Conference (ASPDAC) 2015
9. 共同作者, 共同作者, 共同作者, **學生 A**, 共同作者, and 共同作者, "A Critical-Section-Level Timing Synchronization Approach for Deterministic Multi-Core Instruction-Set Simulations," Design, Automation and Test in Europe Conference (DATE) 2013
10. 共同作者, **學生 A**, 共同作者, "A Non-Intrusive Timing Synchronization Interface for Hardware-Assisted HW/SW Co-Simulation," Design Automation Conference (DAC) 2012
11. 共同作者 , 共同作者 , **學生 A** , 共同作者 , 共同作者, "Analytical Process Scheduling Optimization Using Scaling Factor for Heterogeneous Multi-core Systems", 28th VLSI Design/CAD Symposium, Taiwan, August 2017
12. 共同作者, **學生 A**, 共同作者, 共同作者, "VIRA: A Virtualization-Assisted Approach for Highly Efficient and Accurate Full-System Simulations", 28th VLSI Design/CAD Symposium, Taiwan, August 2017
13. 共同作者, 共同作者, 共同作者, **學生 A**, 共同作者, "A Highly Reliable Fall Detection Approach Using Smart Devices on Real User Self-Adaptive Crowdsourcing-Based Framework," 27th VLSI Design/CAD Symposium, Taiwan, August 2016
14. 共同作者, 共同作者, **學生 A**, 共同作者, "A Highly Accurate Fall Detection Approach Based on Crowdsourcing of Smart Devices," Symposium on Digital Life Technologies 2016
15. 共同作者, 共同作者, **學生 A**, 共同作者, 共同作者, 共同作者 "An Efficient Approach for Synchronization-Function-Level Parallel Multi-Core Instruction-Set Simulations," 26th VLSI Design/CAD Symposium, Taiwan, August 2015

16. 共同作者，共同作者，**學生 A**，共同作者，“An Automatic Timing-Coherent-Based Transactor Generation Approach for Mixed-level Simulations,” 26th VLSI Design/CAD Symposium, Taiwan, August 2015
17. 共同作者，共同作者，共同作者，共同作者，**學生 A**，共同作者，“A Novel Timing Synchronization Approach for Deterministic Multi-Core Instruction-Set Simulations,” 24th VLSI Design/CAD Symposium, Taiwan, August 2013
18. 共同作者，共同作者，共同作者，**學生 A**，and 共同作者，“A Non-Intrusive Timing Synchronization Interface for Hardware-Assisted HW/SW Co-Simulation,” 23rd VLSI Design/CAD Symposium, Taiwan, August 2012
19. 共同作者，**學生 A**，共同作者，共同作者，and 共同作者，“Distributed Scheduling for Parallel Instruction-Set Simulation of Multi-Core Systems,” 22nd VLSI Design/CAD Symposium, Taiwan, August 2011