109 年 2 月　通過 學術審查

年　　級：博 七 （101 博士班入學）

著作列表

Published papers:

Journal Papers

(*)[1] **Hsin-I Wu**, Da-Yi Guo, Ren-Song Tsay, "A Virtualization-Assisted Full-System Simulation Approach for the Verification of System Inter-Component Interactions." IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, (TCAD)
SUBMITTED: 30-Apr-2019
(accept: 2020-02-08)

[2] Jyun-Hao Chang, **Hsin-I Wu,** Hsien-Lun Pai, Ren-Song Tsay, Wai-Kei Mak, "Highly Efficient and Effective Approach for Synchronization-Function-Level Parallel Multicore Instruction-Set Simulations." IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 34.11 (2015): 1822-1835.

Conference Papers

(*) [1] **Hsin-I Wu**, Ren-Song Tsay and Hsu-Hsun Chin, "VIRA: A Virtualization Assisted Deterministic System-Level Simulation," The 35th ACM/SIGAPP Symposium On Applied Computing (SAC 2020)
(*) [2] **Hsin-I Wu**, Chen, Da-Yi Guo, Hsu-Hsun Chin and Ren-Song Tsay, "A Pipleline-Based Scheduler for Optimizing Latency of Convolution Neural Network Inference Over Heterogeneous Multicore Systems," t the 2nd IEEE International Conference on Artificial Intelligence Circuits and Systems. (AICAS 2020)
(*) [3] **Hsin-I Wu**, Chi-Kang Chen, Fong-Yuan Chang, and Ren-Song Tsay, "CORONA: A k-COnnected RObust Interconnection Network Generation Algorithm," The 2020 International Symposium on VLSI Design, Automation and Test (2020 VLSI-DAT)
[4] **Hsin-I Wu**, Chi-Kang Chen, Da-Yi Guo, and Ren-Song Tsay, "A Highly Efficient Virtualization-Assisted Approach for Full-System Virtual Prototypes," Workshop on Synthesis And System Integration of Mixed Information technologies (SASIMI) 2018. Best Paper Award.

[5] Chi-Kang Chen, **Hsin-I Wu**, Cheng-Lin Tsai and Ren-Song Tsay, "A Reuse-Distance Based Approach for Early-Stage Multi-level Cache Design Optimization," Workshop on Synthesis And System Integration of Mixed Information technologies (SASIMI) 2018

[6] **Hsin-I Wu**, Chi-Kang Chen, Tsung-Ying Lu, and Ren-Song Tsay, "A Highly Efficient Full-System Virtual Prototype Based on Virtualization-Assisted Approach," Design, Automation and Test in Europe Conference (DATE) 2018

[7] Chi-Kang Chen, **Hsin-I Wu**, Chi-Ting Hsiao, Ren-Song Tsay, "A Data Effect Aware Microcomponent-Based Estimation Approach for Accurate System-Level Memory Device Power Evaluation," Workshop on Synthesis And System Integration of Mixed Information technologies (SASIMI) 2016, Outstanding Paper Award.

[8] Hsuan-Man Chen, Chi-Kang Chen, **Hsin-I Wu**, Ren-Song Tsay, "An Accurate Crowdsourcing-based Adaptive Fall Detection Approach Using Smart Devices," IEEE International Conference on Healthcare Informatics (ICHI) 2016

[9] Chi-Kang Chen, **Hsin-I Wu**, Chi-Ting Hsiao, and Ren-Song Tsay, "An Accurate and Flexible Early Memory System Power Evaluation Approach Using a Microcomponent Method," International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS) 2016

[11] **Hsin-I Wu**, Li-chun Chen, Ren-Song Tsay, "An Effective Timing-Coherent Transactor Generation Approach for Mixed-level System Simulations," Workshop on Synthesis And System Integration of Mixed Information technologies (SASIMI) 2015

[12] Li-chun Chen, **Hsin-I Wu**, Ren-Song Tsay, "Automatic Timing-Coherent Transactor Generation for Mixed-level Simulations," Asia and South Pacific Design Automation Conference (ASPDAC) 2015

[13] Fan-Wei Yu, Bo-Han Zeng, Yu-Hung Huang, **Hsin-I Wu**, Che-Rung Lee, and Ren-Song Tsay, "A Critical-Section-Level Timing Synchronization Approach for Deterministic Multi-Core Instruction-Set Simulations," Design, Automation and Test in Europe Conference (DATE) 2013

[14] Yu-Hung Huang, **Hsin-I Wu**, Ren-Song Tsay, "A Non-Intrusive Timing Synchronization Interface for Hardware-Assisted HW/SW Co-Simulation," Design Automation Conference (DAC) 2012

[15] Tzu-Yun Huang , Chien-Hao Chen , **Hsin-I Wu** , Chi-Kang Chen , Ren-Song Tsay, "Analytical Process Scheduling Optimization Using Scaling Factor for Heterogeneous Multi-core Systems", 28th VLSI Design/CAD Symposium, Taiwan, August 2017

[16] Bo-Yu Huang, **Hsin-I Wu**, Chi-Kang Chen, Ren-Song Tsay, "VIRA: A Virtualization-Assisted Approach for Highly Efficient and Accurate Full-System Simulations", 28th VLSI Design/CAD Symposium, Taiwan, August 2017.

[17] Kuo-Cheng Chin, Hsuan-Man Chen, Chi-Kang Chen, **Hsin-I Wu**, Ren-Song Tsay, "A Highly Reliable Fall Detection Approach Using Smart Devices on Real User Self-Adaptive Crowdsourcing-Based Framework," 27th VLSI Design/CAD Symposium, Taiwan, August 2016

[18] Hsuan-Man Chen, Chi-Kang Chen, **Hsin-I Wu**, Ren-Song Tsay, "A Highly Accurate Fall Detection Approach Based on Crowdsourcing of Smart Devices," Symposium on Digital Life Technologies 2016

[19] Yun Chang, Jyun-Hao Chang, **Hsin-I Wu**, Hsien-Lun Pai, Ren-Song Tsay, Wai-Kei Mak "An Efficient Approach for Synchronization-Function-Level Parallel Multi-Core Instruction-Set Simulations," 26th VLSI Design/CAD Symposium, Taiwan, August 2015

[20] Hsiang-Yi Wu, Li-Chun Chen, **Hsin-I Wu**, Ren-Song Tsay, "An Automatic Timing-Coherent-Based Transactor Generation Approach for Mixed-level Simulations," 26th VLSI Design/CAD Symposium, Taiwan, August 2015

[21] Fan-Wei Yu, Wen-Jui Lee, Bo-Han Zeng, Yu-Hung Huang, **Hsin-I Wu**, Ren-Song Tsay, "A Novel Timing Synchronization Approach for Deterministic Multi-Core Instruction-Set Simulations," 24th VLSI Design/CAD Symposium, Taiwan, August 2013

[22] Yu-Hung Huang, Ching-Yu Chen, Yi-Shan Lu, **Hsin-I Wu**, and Ren-Song Tsay, "A Non-Intrusive Timing Synchronization Interface for Hardware-Assisted HW/SW Co-Simulation," 23rd VLSI Design/CAD Symposium, Taiwan, August 2012

[23] Meng-Huan Wu, **Hsin-I Wu**, Peng-Chih Wang, Cheng-Yang Fu, and Ren-Song Tsay, "Distributed Scheduling for Parallel Instruction-Set Simulation of Multi-Core Systems," 22nd VLSI Design/CAD Symposium, Taiwan, August 2011, pp. 585~588

Patent

[1] 中華民國專利 I659324， 吳昕益，蕭文菁，電路規劃結果產生方法與系統

[2] 中華民國專利 I657346， 吳昕益，蕭文菁，資料減量及建立資料識別模型的方法、電腦系統及電腦可讀取的記錄媒體

[3] 中華民國專利 M563001， 吳昕益，蕭文菁，壓縮資料識別模型的方法及電腦裝置、電腦可讀取的記錄媒體

[4] 中華民國專利 M570477， 吳昕益，蕭文菁，應用全指數運算於深度神經網路的電腦裝置

[5] 中華民國專利，張瑋鑫、吳昕益，用以備份資料的電腦裝置

Pending

[1] 美國專利，吳昕益，蕭文菁，資料減量及建立資料識別模型的方法、電腦系統及電腦可讀取的記錄媒體

109 年 2 月　通過 學術審查

年　　級：博 三 （104 碩入，106 博入）

著作列表

Journal Papers

1. **Yu-Pei Liang**, Tseng-Yi Chen, Yuan-Hao Chang, Shuo-Han Chen, Hsin-Wen Wei and Wei-Kuan Shih. "B*-sort: Enabling Write-once Sorting Algorithm for Byte-addressable Non-volatile Memory," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD). **(accepted)**
   [CATEGORIES: SCIE, Impact factor = 2.402 (2018), 5 years Impact factor = 2.300]
2. **Yu-Pei Liang,** Tseng-Yi Chen, Yuan-Hao Chang, Shuo-Han Chen, Kam-Yiu Lam, Wei-Hsin Li, and Wei-Kuan Shih, "Enabling Sequential-write-constrained B+-tree Index Scheme to Upgrade Shingled Magnetic Recording Storage Performance," ACM Transactions on Embedded Computing Systems (TECS), volume 18, number 5s, pages 66:1-66:20, October 2019, (Integrated with ACM/IEEE CODES+ISSS'19)
   [CATEGORIES: SCIE, Impact factor = 1.368 (2018), 5 years Impact factor = 1.474]
3. **Yu-Pei Liang,** Shuo-Han Chen, Yuan-Hao Chang, Yong-Chin Lin, Hsin-Wen Wein, and Wei-Kuan Shih, "Mitigating Write Amplification Issue for SMR Drives via the Design of Sequential-Write-Constrained Cache Management," to appear in Elsevier Journal of Systems Architecture (JSA), 99, 101634.
   [CATEGORIES: SCIE, Impact factor = 1.159 (2018), 5 years Impact factor = 1.211]
4. Shuo-Han Chen, Yuan-Hao Chang, **Yu-Pei Liang**, Hsin-Wen Wei, and Wei-Kuan Shih, "An Erase Efficiency Boosting Strategy for 3D Charge Trap NAND Flash," IEEE Transactions on Computers (TC), volume 67, number 9, pages 1246-1258, September 2018.
   [CATEGORIES: SCIE, Impact factor = 3.131 (2018), 5 years Impact factor = 3.237]

Conference Papers

1. **Yu-Pei Liang**, Tseng-Yi Chen, Ching-Ho Chi, Hsin-Wen Wei, and Wei-Kuan Shih, "Enabling a B+-tree-based Data Management Scheme for Key-value Store over SMR-based SSHD," ACM/IEEE Design Automation Conference (DAC), July 2020. (Top Conference)
2. Shuo-Han Chen, **Yu-Pei Liang**, Yuan-Hao Chang, Yun-Fei Liu, Chun-Feng Wu, Hsin-Wen Wei, and Wei-Kuan Shih, "Reinforcing the Energy Efficiency of Cyber-Physical Systems via Direct and Split Cache Consolidation on MLC

STT-RAM," ACM Symposium on Applied Computing (SAC), March 2020.

3. Shuo-Han Chen, **Yu-Pei Liang,** Yuan-Hao Chang, Hsin-Wen Wei and Wei-Kuan Shih, "Boosting the Profitability of NVRAM-based Storage Devices via the Concept of Dual-Chunking Data Deduplication," ACM/IEEE Asia and South Pacific Design Automation Conference (ASP-DAC), January 2020.
4. **Yu-Pei Liang**, Tseng-Yi Chen, Yuan-Hao Chang, Shuo-Han Chen, Kam-Yiu Lam, Wei-Hsin Li, and Wei-Kuan Shih, "Enabling Sequential-write-constrained B+-tree Index Scheme to Upgrade Shingled Magnetic Recording Storage Performance," ACM/IEEE International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS), October 2019, (Top Conference)
5. **Yu-Pei Liang**, Tseng-Yi Chen, Yuan-Hao Chang, Shuo-Han Chen, Pei-Yu Chen and Wei-Kuan Shih. Rethinking Last-level-cache Write-back Strategy for MLC STT-RAM Main Memory with Asymmetric Write Energy. (2019, Jul) 2019 ACM/IEEE International Symposium on Low Power Electronics and Design. (ISLPED 2019) (Top Conference)
6. **Yu-Pei Liang**, Min-Hong Shen, Yi-Han Lien, Wei-Kuan Shih (2019, Feb). Facilitate External Sorting for Large-scale Storage On Shingled Magnetic Recording Drives. Future of Information and Communications Conference. (FICC 2019)
7. **Yu-Pei Liang**, Shuo-Han Chen, Yi-Han Lien, Tseng-Yi Chen, Heng-Yin Chen, Wei-Kuan Shih (2017, Nov). Enabling High-Resolution Video Support for the Next-Generation Internet-Connected Display. 2017 IEEE Cyber Science and Technology Congress (CyberSciTech 2017).
8. Shuo-Han Chen, **Yu-Pei Liang**, Chi-Heng Lee, I-Ju Wang, Wei-Kuan Shih (2017, Feb). Demo Abstract: A Wireless Sensor Network Simulator Focuses on Imitating Wireless Charging Vehicle. The 16th International Conference on Information Processing in Sensor Networks (IPSN'17) , Pittsburgh, Pennsylvania, USA..
9. Shuo-Han Chen, **Yu-Pei Liang**, Yen-Ting Chen, Pei-Yu Chen, Heng-Yin Chen, Wei-Kuan Shih (2017, Feb). Folding State Recognition for Multi-Foldable Mobile Devices . IEEE SoutheastCon 2017, Charlotte, NC, USA.
10. Shuo-Han Chen, Yen-Ting Chen, **Yu-Pei Liang**, Yong-Ching Lin, Heng-Yin Chen, Wei-Kuan Shih (2016, Aug). Improving the Local Disk Cover Algorithm for Placing Relay Nodes in a Wireless Sensor Network. The 2016 International Conference on Collaboration Technologies and Systems (CTS 2016).

Paper under review

1. Chuang, Yi-Jing, Shuo-Han Chen, Yuan-Hao Chang, **Yu-Pei Liang**, Hsin-Wen Wei, Wei-Kuan Shih. DSTL: A Demand-based Shingled Translation Layer for Enabling Adaptive Address Mapping on SMR drives. **Submitted to** ACM Transactions on

Embedded Computing Systems (TECS) **(under major revision)**

2. Shuo-Han Chen, Chih-Hsuan Chen, Tseng-Yi Chen, Yu-Pei Liang, Wei-kuan Shih, Tsan-sheng Hsu. Facilitating External Merge Sort on SMR-based Large-Scale Storage Systems. **Submitted to** Future Generation Computer Systems (FGCS) **(under major revision)**