**110 年 3 月　通過 學術審查**

年　　級：博五（105 入學）

## 著作列表

## Journal Papers

1. Chang-Cheng Ko, **Chia-Chun Lin**, Yung-Chih Chen, and Chun-Yao Wang, "Majority Logic Circuit Minimization Using Node Addition and Removal", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems. (to appear)

2. Xiang-Min Yang, Pei-Pei Chen, Hsiao-Yu Chiang, **Chia-Chun Lin**, Yung-Chih Chen, and Chun-Yao Wang, "LOOPLock 2.0: An Enhanced Cyclic Logic Locking Approach", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems. (to appear)

3. Chia-Cheng Wu, Yi-Hsiang Hu, **Chia-Chun Lin**, Yung-Chih Chen, Juinn-Dar Huang, and Chun-Yao Wang, "Diagnosis for Reconfigurable Single-Electron Transistor Arrays with a More Generalized Defect Model", ACM Journal on Emerging Technologies in Computing System. (to appear)

4. **Chia-Chun Lin**, Chin-Heng Liu, Yung-Chih Chen, and Chun-Yao Wang, "A New Necessary Condition for Threshold Function Identification", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems. pp. 5304-5308, vol. 39, No. 12, December, 2020.

5. Hsiao-Yu Chiang, Yung-Chih Chen, De-Xuan Ji, Xiang-Min Yang, **Chia-Chun Lin**, and Chun-Yao Wang, "LOOPLock : LOgic OPtimization based Cyclic Logic Locking", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems. pp. 2178-2191, vol. 39, No. 10, October, 2020.

6. Chin-Heng Liu, **Chia-Chun Lin**, Yung-Chih Chen, Chia-Cheng Wu, Chun-Yao Wang, and Shigeru Yamashita, "Threshold Function Identification by Redundancy Removal and Comprehensive Weight Assignments", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems. pp. 2284-2297, vol. 38, No. 12, December, 2019.

7. Hsin-Pei Wang, **Chia-Chun Lin**, Chia-Cheng Wu, Yung-Chih Chen, and Chun-Yao Wang, "On Synthesizing Memristor-Based Logic Circuits with Minimal Operational Pulses", IEEE Transactions on Very Large Scale Integration Systems, pp. 2842-2852, vol. 26, No. 12, December, 2018.

## Conference Papers

1. **Chia-Chun Lin**, Hsin-Ping Yen, Sheng-Hsiu Wei, Pei-Pei Chen, Yung-Chih Chen, and Chun-Yao Wang, "A General Equivalence Checking Framework for Multivalued Logic", 2021 IEEE Asia and South Pacific Design Automation Conference.

2. Kit Seng Tam, **Chia-Chun Lin**, Yung-Chih Chen, and Chun-Yao Wang, "An Efficient Approximate Node Merging with an Error Rate Guarantee", 2021 IEEE Asia and South Pacific Design Automation Conference.

3. **Chia-Chun Lin**, Kit Seng Tam, Chang-Cheng Ko, Hsin-Ping Yen, Sheng-Hsiu Wei, Yung-Chih Chen, and Chun-Yao Wang, "A Dynamic Expansion Order Algorithm for the SAT-based Minimization", 2020 IEEE International System-on-Chip Conference.

4. Chun-Jui Chen, Yi-Ting Lin, **Chia-Chun Lin**, Yung-Chih Chen, Yun-Ju Lee, and Chun-Yao Wang, "Rehabilitation System for Limbs using IMUs", 2020 IEEE International Symposium on Quality Electronic Design.

5. Teng-Chia Wang, Yan-Ping Chang, Chun-Jui Chen, Yun-Ju Lee, **Chia-Chun Lin**, Yung-Chih Chen, and Chun-Yao Wang, "IMU-based Smart Knee Pad for Walking Distance and Stride Count Measurement", 2020 IEEE International Symposium on Quality Electronic Design.

6. Ya-Chun Chang, **Chia-Chun Lin**, Yi-Ting Lin, Yung-Chih Chen, and Chun-Yao Wang, "A Convolutional Result Sharing Approach for Binarized Neural Network Inference", 2020 IEEE Design Automation and Test in Europe.

7. Yan-Ping Chang, Teng-Chia Wang, Yun-Ju Lee, **Chia-Chun Lin**, Yung-Chih Chen, and Chun-Yao Wang, "A Smart Single-Sensor Device for Instantaneously Monitoring Lower Limb Exercises", 2019 IEEE International System-on-Chip Conference.

8. De-Xuan Ji, Hsiao-Yu Chiang, **Chia-Chun Lin**, Chia-Cheng Wu, Yung-Chih Chen, and Chun-Yao Wang, "A Glitch Key-Gate for Logic Locking", 2019 IEEE International System-on-Chip Conference.

9. Yung-An Lai, **Chia-Chun Lin**, Chia-Cheng Wu, Yung-Chih Chen, and Chun-Yao Wang, " Efficient Synthesis of Approximate Threshold Logic Circuits with an Error Rate Guarantee", 2018 IEEE Design Automation and Test in Europe.

10. Tung-Yuan Lee, Chia-Cheng Wu, **Chia-Chun Lin**, Yung-Chih Chen, and Chun-Yao Wang, " Logic Optimization with Considering Boolean Relations", 2018 IEEE Design Automation and Test in Europe.

11. **Chia-Chun Lin**, Chiao-Wei Huang, Chun-Yao Wang, and Yung-Chih Chen, " In&Out: Restructuring for Threshold Logic Network Optimization", 2017 IEEE International Symposium on Quality Electronic Design.

## Paper under review

1. **Chia-Chun Lin**, Ciao-Syun Lin, You-Hsuen Tsai, Yung-Chih Chen, and Chun-Yao Wang, " Don't Care Computation and De Morgan Transformation for Threshold Logic Network Optimization", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems.