Department of Computer Science, National Tsing Hua University
Ph.D. Qualification Examination
Operating Systems, Fall 2016

1. (12%) Using Amdahl's Law, calculate the speedup gain of an application that has a 60 percent parallel component for (a) two processing cores and (b) four processing cores.

2. (11%) Consider a system running ten I/O-bound tasks and one CPU-bound task. Assume that the I/O-bound tasks issue an I/O operation once for every millisecond of CPU computing and that each I/O operation takes 10 milliseconds to complete. Also assume that the context-switching overhead is 0.1 millisecond and that all processes are long-running tasks. Describe the CPU utilization for a round-robin scheduler when:
   (a). The time quantum is 1 millisecond
   (b). The time quantum is 10 milliseconds

3. (12%) Consider the following snapshot of a system:

	Allocation	Max
P0	3 0 1 4	5 1 1 7
P1	2 2 1 0	3 2 1 1
P2	3 1 2 1	3 3 2 1
P3	0 5 1 0	4 6 1 2
P4	4 2 1 2	6 3 2 5

   Using the banker's algorithm, determine whether or not each of the following states is unsafe. If the state is safe, illustrate the order in which the processes may complete. Otherwise, illustrate why the state is unsafe.
   (a). Available = (0, 3, 0, 1)
   (b). Available = (1, 0, 0, 2)

4. (8%) What is a privilege instruction? How the privilege instruction can be used to protect a computer system?

5. (9%) Explain why adding more processes into the system cannot improve the CPU utilization when thrashing occurs? Describe one solution in OS that can increase CPU utilization without causing thrashing.

6. (18%) Consider a system using a two-level paging scheme with a 24-bit logical address space, 6-bit outer(first level) page table number, 4 byte page table entries, 1 KB pages, and a 2 entry TLB. The page-table base register access time is 0 ns, TLB access time is 10 ns and memory access time is 100 ns.
   (a). How many address bits are needed for the page offset?
   (b). How much memory in bytes is required to store the inner (second level) page table entirely in main memory?
   (c). The CPU has just been context-switched to a new process whose page tables are entirely stored in main memory. If there is a one-to-one mapping between logical and physical addresses, what is the average effective access time for sequentially accessing the following set of logical addresses (in decimal digits): 2, 100, 56, 2050, 1050, 1500, 2200, 500?
   (d). Suppose the outer page table is stored in main memory starting at frame 0 and the inner page tables are stored in memory sequentially immediately after the outer page table. If logical address B741A5 (in hexadecimal digits) translates to physical address 38ABA5 (in hexadecimal digits), what are the values stored in the corresponding outer page table entry and inner page table entry?

7. (10%) What are the advantages and disadvantages of two methods, namely, linear list and hash table, for implementing a directory for a disk file system?

8. (10%) Describe two methods for handling bad blocks in a hard disk.

9. (10%) Polling and interrupt are two mechanisms for handling interactions between a host and I/O controllers.
   (a). What type of I/O controllers and devices are more suitable for using the polling mechanism? Why?
   (b). What type of I/O controllers and devices are more suitable for using the interrupt mechanism? Why?