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Book Chapter

1. True-to-Life Real-Time Animation of Shallow Water on Today's GPUs.
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2. **Real-Time Ray Tracing with CUDA.**
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   Yung-Feng Chiu and Chun-Fa Chang.
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2. **View-Independent Object-Space Surface Splatting.**
   Chun-Fa Chang, Yung-Feng Chiu and Wei-Zhi Liao.
   IPPR Conference on Computer Vision, Graphics, and Image Processing (CVGIP) 2005 (Citation count: 1).
3. **A Thin-Client Approach for Porting OpenGL Applications to Pocket PC's.**
   Zhe-Yu Lin, Shyh-Haur Ger, Yung-Feng Chiu and Chun-Fa Chang.
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1. **Packet receiving management method and network control circuit with packet receiving management functionality.**
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   US Patent No. 8072997 (Dec 6, 2011).
2. **Apparatus, method, and computer readable medium thereof for drawing 3D water.**
   Yung-Feng Chiu, Chun-Fa Chang, Yu-Jung Cheng.
   US Patent No. 7800612 (Sep. 21, 2010).
3. **Network device and control method thereof.**
   Shang-Chih Chien, Yung-Feng Chiu, Hsiu-Che Chao.
   US Patent Application No. 2011/0122781 (May 26, 2011).
4. **Distributed video stream decoding system on computer and decoding method of the same.**
   Chao-Cheng Li, Chin-Yuan Chiang, Fu-Cheng Wu, Yung-Feng Chiu.
   US Patent No. 7027514 (Apr. 11, 2006).
5. **Apparatus and method for line drawing.**
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   US Patent No. 6891540 (May 10, 2005).
6. **System and method for full-scene anti-aliasing and stereo three-dimensional display control.**
   Yung-Feng Chiu, Hsi-Jou Deng, Ruen-Rone Lee.
   US Patent No. 6690384 (Feb. 10, 2004).
7. **Method and system for eliminating frame tears from an output display.**
   Yung-feng Chiu, Chia-chieh Chen, Yuh-sen Jaw.
   US Patent No. 6597364 (Jul. 22, 2003). (Citation count: 6)

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1. S. H. Chen, Y. L. Lin, Mango C.-T. Chao, “Power-up Sequence Control for MTCMOS Designs,” IEEE Trans. on Very Large Scale Integration (VLSI) Systems, vol. PP, no. 99, pp. 1-11, November 2012.

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1. S. H. Chen, K. C. Chu and J. Y. Lin, “DFM/DFY practices during physical designs for timing, signal integrity, and power,” in Proc. of ASP-DAC, 2007, pp. 232–237.
2. S. H. Chen and J. Y. Lin, “Experiences of low power design implementation and verification,” in Proc. of ASP-DAC, 2008, pp. 742–747.
3. S. H. Chen and J. Y. Lin, “Implementation and Verification Practices of DVFS and Power Gating,” in Proc. of VLSI-DAT, 2009, p.19–22.
4. S. P. Mu, Y. M. Wang, H. Y. Yang, C.-T. Chao, S. H. Chen, “Testing Methods for Detecting Stuck-open Power Switches in Coarse-Grain MTCMOS Designs,” in Proc. of ICCAD, 2010, pp. 155–161.
5. Y. M. Wang, S. H. Chen and Mango C.-T. Chao “An Efficient Hamiltonian-Cycle Power-Switch Routing for MTCMOS Designs,” in Proc. of ASP-DAC, 2012, pp. 59–65.
6. H. W. Hsu, M. L. Chen, H. M. Chen, S. H. Chen, “On Effective Flip-Chip Routing via Pseudo Single Redistribution Layer,” in Proc. of DATE, 2012, pp. 1597–1602.

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1. S. H. Chen, “Verification of Low Power Designs,” in Apache Design, Inc. Silicon Integrity Platform Technical Seminars, Taiwan, 2007.
2. S. H. Chen, “ARM 1176 DVFS Chip Implementation and Verification with CPF, “ in Cadence Design Systems, Inc. CDNLive Conference, Taiwan, 2009. (Best Presentation Award)

3. S. H. Chen, H. K. Chen, “Fast Estimation and Mitigation of Substrate Noise in Early Design Stage for Large Mixed Signal SOCs,” in DAC User Track Sessions, 2010.
4. T. Y. Tsai, Shi-Hao Chen, “A Precise Timing Budgeting Flow for SiP Co-design,” in DAC Track Sessions, 2010.
5. R. J. Lee, H. W. Hsu, H. M. Chen, S. H. Chen, “Implementing the Practical Chip-Package-Board Codesign Considering Package Design and Board Escape Routing,” in DAC WIP Poster, 2011.

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1. S. H. Chen, “System and Method for Power Domain Isolation.” U.S. Patent 7 982 498, May 18, 2010.
2. S. H. Chen, “Apparatus and Methods for Programmable Power-Up Sequence.”, U.S. and C.N. patent pending, Nov. 12, 2009.
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4. S. H. Chen and Y. L. Lin, “Power Booting Sequence Control System and Control Method Thereof.” U.S. and T.W. patent pending, Dec. 6 2010.
5. S. H. Chen, T. Y. Tsai and C. Y. Huang, “Method for Input/Output Design of Chip.” U.S., C.N. and T.W. patent pending, Mar. 16, 2011.
6. S. H. Chen and H.K. Chen, “Tunable Delay Cell Apparatus.” U.S. and T.W. patent pending, Jan. 26, 2011.
7. S. H. Chen and H. K. Chen, “Power Gating for In-rush Current Mitigation.” U.S. and T.W. patent pending, Dec. 2, 2010.

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1. Y. M. Chen and S. H. Chen, “Simultaneous Control of In-rush Current and Dynamic IR Drop in MTCMOS Designs Using Hamiltonian-cycle Routing. ” Chip Design, Internet: http://chipdesignmag.com/display.php?articleId=5128, Mar. 27, 2012 [Apr. 20, 2012].
2. S. H. Chen, “A Novel Systems Approach to Automatically Generating an Interface Rule for Low Power Consumer Application Devices.” Electronic Design, May 7, 2012. (Accepted)

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1. *Ming-Chao Lee*, Hao Yu, Yu-Guan Chen, Yiyu Shi, Shih-Chieh Chang, “On-line Wake-up Scheduling for Multie-Module Designs,” under review in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD).
2. *Ming-Chao Lee*, Yiyu Shi, Shih-Chieh Chang, "Efficient Wakeup Scheduling Considering Both Resource Usage and Timing Budget for Power Gating Designs", accepted in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD). **(SCI, EI)**

3. Da-Cheng Juan, Yu-Ting Chen, *Ming-Chao Lee*, Shih-Chieh Chang, "An Efficient Wake-Up Strategy Considering Spurious Glitches Phenomenon for Power Gating Designs," IEEE Transactions on Very Large Scale Integration Systems (TVLSI), Volume: 18 , Issue: 2, 2010, Page(s): 246 - 255. **(SCI, EI, Impact vector: 0.904, cited by 5)**

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1. *Ming-Chao Lee*, Yu-Guang Chen, Yiyu Shi, Diana Marculescu, Shih-Chieh Chang, "Efficient On-Line Module-Level Wake-Up Scheduling for High Performance Multi-Module Designs," accepted in the International Symposium on Physical Design (*ISPD*), 2012. **(EI)**
2. Kai-Chiang Wu, *Ming-Chao Lee*, Diana Marculescu, Shih-Chieh Chang, "Mitigating Lifetime Underestimation: A System-Level Approach Considering Temperature Variations and Correlations between Failure Mechanisms, " accepted in the Design, Automation & Test in Europe (*DATE*), 2012. **(EI)**
3. Kai-Chiang Wu, Diana Marculescu, *Ming-Chao Lee*, Shih-Chieh Chang, "Analysis and Mitigation of NBTI-Induced Performance Degradation for Power-Gated Circuits," Proc. on the International Symposium on Low Power Electronics and Design (*ISLPED*), 2011, Page(s): 139 - 144. **(EI, cited by 1)**
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5. *Ming-Chao Lee*, Yu-Ting Chen, Yo-Tzu Cheng, Shih-Chieh Chang, "An efficient wakeup scheduling considering resource constraint for sensor-based power gating designs," Proc. on the International Conference on Computer Aided Design (*ICCAD*), 2009, Page(s): 457 - 460. **(EI, cited by 5)**
6. *Ming-Chao Lee*, Shih-Chieh Chang, Chun-Sung Su, Tsai, E., "Performance and wake-up schedule optimization of power gating design," Proc. of the International SoC Design Conference (*ISOCC*), 2008, Volume: 01, Page(s): I-36 - 39. **(EI, cited by 1)**
7. Yu-Ting Chen, Da-Cheng Juan, *Ming-Chao Lee*, Shih-Chieh Chang, "An efficient wake-up schedule during power mode transition considering spurious glitches phenomenon," Proc. on the International Conference on Computer Aided Design (*ICCAD*), 2007, Page(s): 779 - 782. **(EI, cited by 17)**

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2. Synthesis of an Efficient Controlling Structure for Post-Silicon Clock Skew Minimization," Proc. of International Conference on Computer Aided Design, ICCAD, pp. 746-749, 2010. (EI, accepted paper:108, rate= 30%, **citation number = 2**) **Mac Y.C. Kao**, H.M. Chou, K.T. Tsai, and S.C. Chang, "

3. A Robust Architecture for Post-Silicon Skew Tuning," Proc. of International Conference on Computer Aided Design, ICCAD, Nov. 2011. (EI, accepted paper:106, rate= 30%, **citation number = 1**) **Mac Y.C. Kao**, K.T. Tsai, and S.C. Chang, "

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Books and Book Chapters:

B1) **Chiao-Ling Lung**, Jui-Hung Chien, Yung-Fa Chou, Ding-Ming Kwai, and Shih-Chieh Chang, "Three-dimensional Integrated Circuits Design for Thousand-core Processors: from Aspect of Thermal Management," a chapter of the book "*VLSI Design*", InTech, Jan 2012 (ISBN: 979-953-307-884-7)

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J1) **Chiao-Ling Lung**, Yu-Shih Su, Shih-Hsiu Huang, Yiyu Shi, and Shih-Chieh Chang, "Fault-Tolerant Clock Networks for 3D ICs," under reviewed by *IEEE Transactions on on Computer-Aided Design of Integrated Circuits and Systems* (*TCAD*)

J2) **Chiao-Ling Lung**, Huai-Chung Chang, Ding-Ming Kwai, and Shih-Chieh Chang, "Thermal-driven Task Allocation for 3D Multi-core Processor," in *Information and Communications Research Laboratories Journal 141th*, pp. 19-27, Oct. 2011

J3) Yu-Shih Su, **Chiao-Ling Lung**, and Shih-Chieh Chang, "TSV Fault-tolerant Unit for 3-D Clock Network," in *Information and Communications Research Laboratories Journal 141th*, pp. 28-35, Oct. 2011.

J4) Jui-Hung Chien, **Chiao-Ling Lung**, Huai-Chung Chang, and Ding-Ming Kwai, "Design and Realization of Virtual Multi-core Based Thermal Test Chip," in *Information and Communications Research Laboratories Journal 141th*, 11-18, Oct. 2011.

J5) **Chiao-Ling Lung**, and Ji-Jan Chen, "Improvement of Gate-level Low Power Design Methodology," *System-on-a-Chip Technical Journal 5th*, pp. 120-136, Oct. 2007. (cited by **3**[1])

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C1) Jui-Hung Chien, Hao Yu, Nien-Yu Tsai, **Chiao-Ling Lung**, Chin-Chi Hsu, Yung-Fa Chou, Ping-Hei Chen, Shih-Chieh Chang, and Ding-Ming Kwai, "Hybrid Thermal Solution for 3D-ICs: Using Thermal TSVs with Placement Algorithm for Stress Relieving Structures," *in* ***Proc. of International Conference on Electronic Components and Technology Conference, ECTC***, pp. 1455-1460, San Diego, CA., USA., May 2012.

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C2) **Chiao-Ling Lung**, Jui-Hung Chien, Yiyu Shi, and Shih-Chieh Chang, "TSV Fault-tolerant Mechanisms with Application to 3D Clock Networks," in *Proc.*

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of International SoC Design Conference, ISOCC, pp. 127-130,Jeju, Korea, Nov. 2011.

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C3) Jui-Hung Chien, **Chiao-Ling Lung**, Ta-Wei Lin, Kun-Ju Tsai, Ting-Sheng Chen, Yung-Fa Chou, Ping-Hei Chen, Shih-Chieh Chang, and Ding-Ming Kwai, "Design and Implementation of 3D-thermal Test Chip for Exploration of Package Effects," in *Proc. of International Conference on Microsystems Packaging Assembly and Circuits Technology Conference, IMPACT,* pp. 260-263,Taipei, Taiwan, Oct. 2011.

- EI; **Best Paper Award**

C4) **Chiao-Ling Lung**, Yu-Shih Su, Shih-Hsiu Huang, Yiyu Shi, and Shih-Chieh Chang, "Fault-tolerant 3D Clock Network," *in **Proc. of Design Automation Conference, DAC***, pp. 645-651, San Diego, CA., USA., June 2011.

- EI; **Cited by 1**
- **Acceptance rate** of oral presentation: 156/690 = **22.6%**

C5) Jui-Hung Chien, **Chiao-Ling Lung**, Kun-Ju Tsai, Chin-Chi Hsu, Ting-Sheng Chen, Yung-Fa Chou, Ping-Hei Chen, Shih-Chieh Chang, and Ding-Ming Kwai, "Realization of 3-dimentional Virtual 126-core System with Thermal Sensor-network Using Metallic Thermal Skeletons," *in **Proc. of International Conference on Electronic Components and Technology Conference, ECTC***, pp. 873-879, Lake Buena Vista, FL., USA., June 2011.

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C6) Shan-Chien Fang, Chia-Chien Weng, Chun-Kai Tseng, Chen-Wei Hsu, Jia-Lu Liao, Shi-Yu Huang, **Chiao-Ling Lung**, and Ding-Ming Kwai, "SoC Power Analysis Framework and Its Application to Power-thermal Co-simulation," in *Proc. of International Symposium on VLSI Design Automation and Test, VLSI-DAT*, pp. 1-4, Hsinchu, Taiwan, April 2011.

- EI; **Cited by 1**

C7) **Chiao-Ling Lung**, Yu-Shih Su, Shih-Hsiu Huang, Yiyu Shi, and Shih-Chieh Chang, "Robust 3D Clock Scheme," in *ACM International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems (TAU Workshop)*, Santa Barbara, CA., USA., March 2011.

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C8) **Chiao-Ling Lung**, Yi-Lun Ho, Ding-Ming Kwai, and Shih-Chieh Chang, "Thermal-aware On-line Task Allocation for 3D Multi-core Processor Throughput Optimization," in ***Proc. of Design, Automation & Test in Europe, DATE***, pp. 1-6, Grenoble, France, March 2011.

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C9) **Chiao-Ling Lung**, Yi-Lun Ho, Shih-Hsiu Huang, Chen-Wei Hsu, Jia-Lu Liao, Si-Yu Huang, and Shih-Chieh Chang, "Thermal Analysis Experiences of a Tri-core SoC System," in *Proc. of International Conference on Green Circuits and Systems, ICGCS,* pp. 589-594, Shanghai, China, June 2010.

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- EI; **Cited by 7**

C11) **Chiao-Ling Lung**, Hai-Chi Hsiao, Zi-Yi Zeng, and Shih-Chieh Chang, "LP-based Multi-mode Multi-corner Clock Skew Optimization," in *Proc. of International Symposium on VLSI Design Automation and Test, VLSI-DAT*, pp. 335-338, Hsinchu, Taiwan, April 2010.

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C12) **Chiao-Ling Lung**, Zi-Yi Zeng, Chung-Han Chou, and Shih-Chieh Chang, "Clock Skew Optimization Considering Complicated Power Modes," in ***Proc. of Design, Automation & Test in Europe, DATE***, pp. 1474-1480, Dresden, Germany, March 2010.

- EI; **Cited by 9**
- **Acceptance rate** of oral presentation: 156/847 = **18.4%**

C13) **Chiao-Ling Lung**, "Low Power Emphasized PAC DSP Implementation," *Synopsys User Group, SNUG*, Hsinchu, Taiwan, May 2007.

- **Best User Session**

C14) **龍巧玲**, 陳繼展, "閘級層次低功率實現技術之改善," 電子工程專輯, June 2007.

C15) **Chiao-Ling Lung**, "Low Power Design Methodology and Implementation," SoCTEC 4th, Dec. 2006

C16) Jin-Tai Yan, **Chiao-Ling Lung**, and Chao-Hung Lu, "Optimal Wire Sizing for DME-based Zero-skew Clock Routing," in *Proc. of* VLSI Design /CAD Symposium, Aug. 2003

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P1) 蒯定明, 周永发, **龙巧玲**, and 钱睿宏, "半导体元件堆叠结构," *filing to CN patent*, 201210111141.1, April 16, 2012.

P2) Ding-Ming Kwai, Yung-Fa Chou, **Chiao-Ling Lung**, and Jui-Hung Chien, "Semiconductor Device Stacked Structure," *pending to US patent*, 13/450,482, April 19, 2012.

P3) 蒯定明, 周永發, **龍巧玲**, and 錢睿宏, "半導體元件堆疊結構," *pending to ROC patent*, 100147767, Dec. 21, 2011.

P4) **龙巧玲**, 苏佑世, 史弋宇, and 张世杰, "硅通孔的容错单元与方法," *filing to CN patent*, 201110196863.7, July 28, 2011.

P5) **龍巧玲**, 蘇祐世, 史弋宇, and 張世杰, "貫矽導孔的容錯單元與容錯方法," *filing to ROC patent*, 100120191, June 14, 2011.

P6) **Chiao-Ling Lung**, Yu-Shih Su, Yiyu Shi, and Shih-Chieh Chang, "Fault-tolerant Unit and Fault-tolerant method for Through-silicon Via," *filing to US patent*, 13/236,661, March 30, 2011.

P7) **Chiao-Ling Lung**, and Shih-Chieh Chang, "Power-mode-aware Clock Tree and Synthesis Method thereof," US 8,179,181 B2, May. 15, 2012.

P8) **龍巧玲**, and 張世杰, "具電源模式感知之時脈樹及其合成方法," 201118526, Nov. 20, 2009.

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T1) **Chiao-Ling Lung**, “3D Thermal Test Chip Design – Observation and Study of Thermal Effects and Thermal TSVs,” 3D IC Special Interest Group-3D IC Forum, Hsinchu, Taiwan, Oct. 2010.

T2) **Chiao-Ling Lung**, “Introduction of 3D Integration,” National Tsing Hua University, Hsinchu, Taiwan, June 2010.

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1. 共同作者，**A君**，共同作者，共同作者，and共同作者，"GPU Performance Enhancement via Communication Cost Reduction," Special Issue of *The International Journal of Future Generation Computer Systems* (FGCS). (invited)

2. **A君**, 共同作者, 共同作者, and Y共同作者, "PBIG: Optimizing Pairwise Box Intersection Computation on GPUs for Large-Scale Simulations," *ACM Transactions on Modeling and Computer Simulation* (TOMACS). (revision)

3. **A君**，共同作者，共同作者，and共同作者，"Synchronization on GPUs: Performance Curse or Blessing?," *IEEE Transactions on Parallel and Distributed Systems* (TPDS). (submitted)

4. **A君**, 共同作者, 共同作者, and共同作者, "Data Compression for Performance on GPUs: A Case Study of Rectangle Intersection Problem," *The Journal of SuperComputing* (JOS). (submitted)

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1. 共同作者，**A君**，共同作者，共同作者，and共同作者，"GPU Performance Enhancement via Communication Cost Reduction: Case Studies of Radix Sort and WSN Relay Node Placement Problem," accepted by *the 12th IEEE/ACM International Symposium on Cluster, Cloud, and Grid Computing* (**CCGRID** 2012).

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3. **A君**, 共同作者, 共同作者, and共同作者, "A Parallel Rectangle Intersection Algorithm on GPU+CPU," *Proceedings of the 11th IEEE/ACM International Symposium on Cluster, Cloud, and Grid Computing* (**CCGRID** 2011), pp. 43-52.

4. **A君**, 共同作者and共同作者, "Offloading Region Matching of Data Distribution Management with CUDA," *Proceedings of IEEE International Conference on Intelligent Systems, Modeling and Simulation* (ISMS 2010), pp. 306-311.

5. 共同作者, 共同作者, **A君**, and共同作者, "A Scalable HLA RTI System Based on Multiple-FedServ Architecture," *Proceedings of IEEE International Conference on Computer Modeling and Simulation* (UKSIM 2010), pp. 527-532.

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7. **A君**, 共同作者, and共同作者, "Cooperative Localization with Pre-Knowledge using Bayesian Network for Wireless Sensor Networks," *Proceedings of IEEE ICPP Workshops* 2007 (ICPPW 2007).

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2. **B君**, 共同作者, 共同作者, 共同作者, and共同作者, "A Self-Adaptive Resource Index and Discovery System in Distributed Computing Environments," *to appear in International Journal of Ad Hoc and Ubiquitous Computing*, 2012.
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4. **B君**, 共同作者, 共同作者, 共同作者, and共同作者, "G2G: A Meta-Grid Framework for the Convergence of P2P and Grids," *International Journal of Grid and High Performance Computing*, vol. 2, no. 3, 2010, pp. 1-16.
5. **B君** and共同作者, "A New Mechanism for Resource Monitoring in Grid Computing," *Future Generation Computer Systems,* vol. 25, no. 1, 2009, pp. 1-7.

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1. **B君**, 共同作者, 共同作者, 共同作者, and共同作者, "Direction-Aware Resource Discovery Service in Large-Scale Grid and Cloud Computing," to appear in *2011 IEEE International Conference on Service-Oriented Computing and Applications* (*SOCA*), Irvine, CA, USA, 2011.
2. 共同作者, **B君**, 共同作者, 共同作者, and共同作者, "A Novel Approach for Cooperative Overlay-Maintenance in Multi-overlay Environments," in *2010 IEEE Second International Conference on Cloud Computing Technology and Science* (*CloudCom*), Indianapolis, Indiana, USA, 2010, pp. 81-88.
3. 共同作者, **B君**, 共同作者, 共同作者, and共同作者, "SARIDS: A Self-Adaptive Resource Index and Discovery System," in *10th International Symposium on Pervasive Systems, Algorithms, and Networks* (*I-SPAN*), Kaohsiung, Taiwan, 2009, pp. 521-526.
4. **B君**, 共同作者, 共同作者, 共同作者, and共同作者, "G2G: A Meta-Grid Framework for the Convergence of P2P and Grids," in *Proceedings of the 4th International Conference on Advances in Grid and Pervasive Computing (GPC*), *Lecture Notes In Computer Science (LNCS*), Geneva, Switzerland, 2009, pp. 131-141.