105 年 3 月　通過 學術審查

年　　級：博六 （98 碩入，99 上直升）

著作列表

Journal Papers

1. **Ching-Yi Huang**, Yun-Jui Li, Chian-Wei Liu, Chun-Yao Wang, Yung-Chih Chen, Suman Datta, and Vijaykrishnan Narayanan, “Diagnosis and Synthesis for Reconfigurable Single-Electron Transistor Arrays,” *IEEE Transactions on Very Large Scale Integration Systems (IEEE TVLSI)*, 2016. (SCI, impact factor = 1.356)

2. **Ching-Yi Huang**, Zheng-Shan Yu, Yung-Chun Hu, Tung-Chen Tsou, Chun-Yao Wang, and Yung-Chih Chen, “Correctness Analysis and Power Optimization for Probabilistic Boolean Circuits," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (IEEE TCAD)*, pp. 615-625, April, 2015. (SCI, impact factor = 1.003)

3. Chian-Wei Liu, Chang-En Chiang, **Ching-Yi Huang**, Yung-Chih Chen, Chun-Yao Wang, Suman Datta, Vijaykrishnan Narayanan, “Synthesis for Width Minimization in the Single-Electron Transistor Array," *IEEE Transactions on Very Large Scale Integration Systems (IEEE TVLSI)*, pp. 2862-2875, December, 2015. (SCI, impact factor = 1.356)

4. Yung-Chih Chen, Chun-Yao Wang, and **Ching-Yi Huang**, “Verification of Reconfigurable Binary Decision Diagram-based Single-Electron Transistor Arrays," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (IEEE TCAD)*, pp.1473-1483, October 2013. (SCI, impact factor = 1.003)

5. Tai-Lin Chen, Chun-Yao Wang, **Ching-Yi Huang**, and Yung-Chih Chen, “An Efficient Interpolation-based Projected Sum of Product Decomposition via Genetic Algorithm," *Journal of Multiple-Valued Logic and Soft Computing (JMVLSC)* (to appear). (SCI, impact factor = 0.346)

6. Ching-Hsuan Ho, Yung-Chih Chen, Chun-Yao Wang, **Ching-Yi Huang**, Suman Datta, and Vijaykrishnan Narayanan, "Area-aware Decomposition for Single-Electron Transistor Arrays," *ACM Transactions on Design Automation of Electronic Systems (ACM TODAES)* (to appear). (SCI, impact factor = 0.686)

7. Chen-Yu Lin, Yung-Chih Chen, Chun-YaoWang, **Ching-Yi Huang**, and Chiou-Ting Hsu, "Minimization of Number of Neurons in Voronoi Diagram-based Artificial Neural Networks," *IEEE Transactions on Multi-Scale Computing Systems (IEEE TMSCS)*, under major revision. (SCI)

Conference Papers

1. **Ching-Yi Huang**, Chian-Wei Liu, Chun-Yao Wang, Yung-Chih Chen, Suman Datta and Vijaykrishnan Narayanan, "A Defect-aware Approach for Mapping Reconfigurable Single-Electron Transistor Arrays," *2015 Asia and South Pacific Design Automation Conference (ASP-DAC)*, pp. 118-123, January 2015. (EI, Acceptance rate: 108/318, 33.9%)

2. **Ching-Yi Huang**, Daw-Ming Lee, Chun-Chi Lin, and Chun-Yao Wang, "Error Injection & Correction: An Efficient Formal Logic Restructuring Algorithm," *2012 International SoC Design Conference (ISOCC)*, pp. 188-191, November 2012. (EI, Acceptance rate: 59%)

3. Yu-Min Chou, Yung-Chih Chen, Chun-Yao Wang, and **Ching-Yi Huang**, "MajorSat: A SAT Solver to Majority Logic," *2016 Asia and South Pacific Design Automation Conference (ASP-DAC)*, pp. 480-485, January 2016. (EI)

4. Jui-Hung Chen, Yung-Chih Chen, Wan-Chen Weng, **Ching-Yi Huang**, and Chun-Yao Wang, 'Synthesis and Verification of Cyclic Combinational Circuits," *2015 IEEE International System-on-Chip Conference (SOCC)*, pp. 257-262, September 2015. (EI)

5. Wan-Chen Weng, Yung-Chih Chen, Jui-Hung Chen, **Ching-Yi Huang**, and Chun-Yao Wang, "Using Structural Relations for Checking Combinationality of Cyclic Circuits," *2015 Design, Automation and Test in Europe Conference and Exhibition (DATE)*, pp. 325-328, March 2015. (EI)

6. Chian-Wei Liu, Chang-En Chiang, **Ching-Yi Huang**, Chun-Yao Wang, Yung-Chih Chen, Suman Datta, and Vijaykrishnan Narayanan, "Width

Minimization in the Single-Electron Transistor Array Synthesis," *2014 Design, Automation and Test in Europe Conference and Exhibition (DATE)*, March 2014. (EI)

7. Chia-Chun Lin, Chun-Yao Wang, Yung-Chih Chen, and **Ching-Yi Huang**, "Rewiring for Threshold Logic Circuit Minimization," *2014 Design, Automation and Test in Europe Conference and Exhibition (DATE)*, March 2014. (EI)

8. Chen-Kuan Tsai, Chun-Yao Wang, **Ching-Yi Huang**, and Yung-Chih Chen, "Sensitization Criterion for Threshold Logic Circuits and its Application," *2013 IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, pp. 226-233, November 2013. (EI)

9. Yen-Chi Yang, Chun-Yao Wang, **Ching-Yi Huang** and Yung-Chih Chen, "Pattern Generation for Mutation Analysis Using Genetic Algorithms," *2013 International Symposium on Circuits and Systems (ISCAS)*, pp. 2545-2548, May 2013. (EI)

10. Chang-En Chiang, Li-Fu Tang, Chun-Yao Wang, **Ching-Yi Huang**, Yung-Chih Chen, Suman Datta and Vijaykrishnan Narayanan, "On Reconfigurable Single-Electron Transistor Arrays Synthesis Using Reordering Techniques," *2013 Design, Automation and Test in Europe Conference and Exhibition (DATE)*, pp. 1807-1812, March 2013. (EI)

11. Hsiu-Yi Lin, Chun-Yao Wang, Shih-Chieh Chang, Yung-Chih Chen, Hsuan-Ming Chou, **Ching-Yi Huang**, Yen-Chi Yang, and Chun-Chien Shen, "A Probabilistic Analysis Method for Functional Qualification under Mutation Analysis," *2012 Design, Automation and Test in Europe Conference and Exhibition (DATE)*, pp. 147-152, March 2012. (EI)

12. Pin-Yi Kuo, Chun-Yao Wang, and **Ching-Yi Huang**, "On Rewiring and Simplification for Canonicity in Threshold Logic Circuits," *2011 IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, pp. 396-403, November 2011. (EI)

13. Yen-An Chen, Chun-YaoWang, **Ching-Yi Huang**, and Hsiu-Yi Lin, "A Register-Transfer Level Testability Analyzer," *2011 IEEE International SOC Conference (SOSS)*, pp. 219-224, September 2011. (EI)